IN THE SPECIFICATION:

Please rewrite the paragraph at page 4, lines 12 to page 5, line 5, so that it reads as follows:

Referring to FIG. 3 showing a schematic view illustrating a layout of the flash memory according to the invention, the layout comprises a diffusion region 52 in a memory cell array region 50; a buried diffusion layer 54 extended across the diffusion region 52; a select transistor region 60 having polysilicon gates 62 and 64, which are parallel to each other and perpendicularly extended toward a direction of the cell memory array region 50; a metal wire 70 extended from the memory cell array region 50 to one side of the polysilicon gate 62, passed through the contact windows 65 and 66, and connected to the buried diffusion layer 54 and a source of a select transistor 69; and a metal wire 72 extended between the polysilicon gates 62 and 64, passed through the contact window 68, and connected to a drain of the select transistor 69. The buried diffusion layer 54 is for serving as a bit line of the memory cells. The polysilicon gates 62 and 64 input voltages through contact windows 74 and 76, so as to control conductance of corresponding select transistors (e.g., the select transistor 69 and a select transistor 69' that is coupled to the memory cell array region 50 by a wire 70' that is shown only schematically) to further select specific memory cells for access. The contact windows 74 and 76 are disposed in opposition for reducing an area occupied by the select transistors.